IN THE SPECIFICATION

Please delete the entire Summary of the Invention which begins on page 4, line 1 and ends on page 5, line 25.

Please amend the paragraph on page 6, lines 8-9 as follows:

~~Figure 2~~ **Figure 2A and 2B** illustrate one embodiment in which logic is programmably coupled to the megacell.

Please amend the paragraph on page 8, lines 11-19 as follows:

One embodiment of the programmable bus system is illustrated in ~~Figure 2~~ **Figures 2A and 2B**. The system is illustrated using a megacell circuit; however, it is readily apparent that the system can be utilized with a variety of types of circuits and/or components. The type of megacell component used in the following discussion is a 256x8 dual port static random access memory (SRAM). However, the bus system described herein is not limited to SRAM components. A variety of components, such as microcontrollers, buffers, digital signal processors (DSPs) can be coupled to the bus system described herein.

Please amend the paragraph on page 8, line 20, through page 9, line 9 as follows:

~~Figure 2~~ **Figures 2A and 2B** illustrate one embodiment of the configurable bus system of the present invention. Referring to ~~Figure 2~~ **Figures 2A and 2B**, the configurable bus system of lines includes groups of lines 210, lines 215, and lines 220, 225. Each data input/output port of the megacell 205 is connected to one line of lines 210. For example, DI[0] is connected to Data[0], DI[1] is connected to Data[1], etc. In addition, each read or write address port of the megacell 205 is connected to one of the group of lines 215. Furthermore, lines 225 are connected to the control ports of the megacell 205. It is recognized that the exemplary system described herein has been programmed to convey address, data and control information across certain of the lines which form the bus system of lines. It is readily apparent that in other applications the

system may only convey other combinations of information such as data and control. In addition, one skilled in the art recognizes that the lines are programmable and can be configured for a variety of types of information in addition to the types of information described herein.

Please amend the paragraph on page 9, line 10, through page 10, line 2 as follows:

In the present embodiment, data is preferably input to the megacell 205 and output from the megacell through interface logic 230. As will be described below, the interface logic is embodied in a programmable logic device, such as a field programmable gate array (FPGA); however, other types of logic can be used. A first set of programmable connections programmably couple the interface logic 230 to the data input/output ports of the megacell 205 (e.g., elements 235, 240, 245, 250). For example, programmable elements 235, 240 selectively connect a first line 255 from the interface logic 230 to lines Data[0] 211 and Data[8] 212. In addition, in the present embodiment, the programmable elements of the first set of programmable elements programmably couple the interface logic 230 to line 215. For example, programmable elements 237, 247 selectively connect a first line 256 from the input/output logic 230 to bussed lines READA[0] 216 and WRITEA[0] 217. Furthermore, the location of the programmable elements and the lines that each programmable element selectively connect to can be varied according to application. ~~Figure 2~~ **Figure 2A and 2B** illustrate one arrangement of programmable elements of the first set of programmable elements that provides flexibility in configuring the bus system of lines.